REMARKS

Claims 1-3, 5, 7-11, 13, and 15 are pending after the amendments. Claims 1-14 were previously pending. Claims 4, 6, 12, and 14 are cancelled and their limitations have been merged into their parent claims. Claim 15 is added. Support for Claim 15 is found in the emitter follower of Fig. 6.

The claims have been amended to clarify that the current source provides a fixed current, as opposed to the current source being a switching transistor. The fact that the current source is fixed is conveyed to one skilled in the art in the various circuit diagrams, in the waveform of Fig. 5, and in the equation on page 4, line 16, where I_o is a fixed value used to calculate Riso. Independent Claims 1 and 9 have also been amended to recite basically the structure on the left hand side of Fig. 7 where the isolation resistors Riso1 and Rios2 are below the Riso5. This is a very important distinguishing feature, as described below.

A key aspect of the circuits of Claims 1 and 9 is that isolation resistors Riso1 and Rios2 cause the switching signal from the switching transistor to not be significantly distorted by the in-rush current into the capacitance between each isolation resistor and its fixed current source. If the current source were another switching transistor, the claimed circuit would not make sense.

The examiner rejected Claims 1, 3, 4, 6, 8, 9, 11, 12, and 14 as being anticipated by Sasamura's Fig. 1. In Sasamura's Fig. 1, the resistor 28 is used to set the gain of the amplifier (see equation 5). It is vital that the ballast resistors 24 and 26 not be connected below resistor 28 or else resistor 28 could not be used to set the gain in accordance with equation 5. Resistors 24 and 26 are used to offset some of the mismatch between transistors 12 and 14.

In contrast, Applicant's Claim 1 includes the limitation of "a second isolation resistor [Riso5 in Fig. 7] coupled in series directly between the first current carrying terminal of the first switching transistor and the second current carrying terminal of the second switching transistor." Accordingly, Claim 1 is not anticipated by Sasamura.

It is not obvious to modify Sasamura's Fig. 1 to be like Applicant's Claim 1 because the Sasamura circuit would not operate properly. Sasamura needs the ballast resistors 24 and 26 above the resistor 28 in order for the resistors 24 and 26 to function as intended and in order for resistor 28 to set the gain (eq. 5).

Independent Claim 9 has similar limitations regarding the "second isolation resistor" so is also patentable over Sasamura. The remaining claims, except Claim 15, are dependent on Claim 1 or 9.

The examiner also indicated that the independent claims were anticipated by Takahashi's Fig. 6. Takahashi has no fixed current sources, in contrast to Applicant's Claims 1 and 9, and the amplifier is a symmetrical switching amplifier. The resistors 39 and 40 are not isolation resistors. Accordingly, Takahashi does not anticipate Claims 1 and 9. Takahashi does not render Claims 1 and 9 obvious because Takahashi's resistor configuration is a result of the symmetrical switching arrangement. If the bottom PNP transistors were fixed current sources, like in Applicant's claims, Takahashi's resistor configuration would make no sense. Accordingly, it is not obvious to modify the Takahashi circuit to be the same as Applicant's claimed circuit.

The examiner also indicated that the independent claims were anticipated by Quinn's Fig. 3A. Quinn's Fig. 3A has current sources 82, 84, 108, and 110. The current sources are not connected to the switching transistors through resistors as recited in Applicant's Claims 1 and 9. Quinn's circuit is very different from Applicant's claimed circuit in many ways and could not make Applicant's circuit obvious.

The examiner also indicated that the independent claims were anticipated by Murden's Fig. 3. Murden's Fig. 3 does not have the claimed second isolation resistor coupled directly between the current carrying terminals of a switching pair of transistors and is different for other reasons. The Murden circuit does not anticipate or make obvious Applicant's claims.

Accordingly, Claims 1-3, 5, 7-11, and 13 are patentable over the cited art.

Independent Claim 15 recites the emitter follower configuration of Applicant's Fig. 6 where the output is taken at the emitter. None of the cited prior art circuits is an emitter follower circuit much less an emitter follower circuit using the isolation resistor. Accordingly, Claim 15 is also patentable.

Should the Examiner have any questions, the Examiner is invited to call the undersigned at (408) 382-0480.

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Signature 6/23/05 Date

Respectfully submitted,

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